Please delete page 2, line 22.

Please replace paragraph **[0008]** as follows:

[0008] One exemplary embodiment of the present invention is a piezoelectric device including a semiconductor integrated circuit and a piezoelectric resonator element both included in a package, wherein an opening is formed in the center of a base provided with an input/output electrode pattern, the semiconductor integrated circuit is mounted in the center of the opening, and the semiconductor integrated circuit is connected to the electrode pattern on the base through a plurality of bumps.

Please replace paragraph **[0009]** as follows:

[0009] In another exemplary embodiment of the present invention, in the piezoelectric device described above, the plurality of bumps formed on the semiconductor integrated circuit are formed at regular intervals on the center portion of an active element surface of the semiconductor integrated circuit.

Please replace paragraph **[0010]** as follows:

[0010] In another exemplary embodiment of the present invention, in the piezoelectric device described above, the plurality of bumps formed on the semiconductor integrated circuit are concentrically formed about the center of an active element surface of the semiconductor integrated circuit.

Please replace paragraph **[0011]** as follows:

[0011] In another exemplary embodiment of the present invention, in the piezoelectric device described above, a dummy bump is formed on the active element surface of the semiconductor integrated circuit.

Please replace paragraph **[0012]** as follows:

[0012] In another exemplary embodiment of the present invention, in the piezoelectric device described above, the dummy bump formed on the semiconductor integrated circuit is connected to the electrode pattern on the base.

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Please replace paragraph **[0013]** as follows:

[0013] In another exemplary embodiment of the present invention, the piezoelectric device described above further includes a layered part, which surrounds the semiconductor integrated circuit, for mounting the piezoelectric resonator, the layered part including at least two layers, including a first layer and a second layer, wherein an opening of the first layer is formed to be larger than an opening of the second layer.

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Please replace paragraph **[0014]** as follows:

[0014] In another exemplary embodiment of the present invention, in the piezoelectric device described above, each of the plurality of bumps formed on the semiconductor integrated circuit is shaped to have two levels, one having a diameter 0.8 to 0.9 times and the other having a diameter 0.4 to 0.45 times the length of a side of an opening in a pad provided on an active element surface of the semiconductor integrated circuit.

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Please replace paragraph **[0015]** as follows:

[0015] In another exemplary embodiment of the present invention, in the piezoelectric device described above, the base may consist of a ceramic composite substrate.

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Please replace paragraph **[0016]** as follows:

[0016] In another exemplary embodiment of the present invention, in the piezoelectric device described above, each of the plurality of bumps formed on the semiconductor integrated circuit is an Au bump.

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Please replace paragraph **[0017]** as follows:

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[0017] In another exemplary embodiment of the present invention, in the piezoelectric device described above, a protrusion is formed in at least one side wall of the base facing the side of the semiconductor integrated circuit.

Please replace paragraph **[0018]** as follows:

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[0018] In another exemplary embodiment of the present invention, in the piezoelectric device described above, the protrusion is formed in each of the side walls of the base facing the two sides along the longitudinal direction of the semiconductor integrated circuit.

Please replace paragraph **[0019]** as follows:

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[0019] In another exemplary embodiment of the present invention, in the piezoelectric device described above, the protrusion formed in the side wall of the base has substantially the same height as, or is higher than, the semiconductor integrated circuit.

Please replace paragraph **[0020]** as follows:

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[0020] In another exemplary embodiment of the present invention, in the piezoelectric device described above, a gap between the protrusion formed in the side wall of the base and the semiconductor integrated circuit is set to a range between 0.05 and 0.15 mm.

Please replace paragraph **[0021]** as follows:

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[0021] Another exemplary embodiment of the present invention is a piezoelectric device including a semiconductor integrated circuit and a piezoelectric resonator element included in a package, wherein an opening is formed in the center of a base provided with an input/output electrode pattern, a plurality of bumps are formed at two opposing sides of an active element surface of the semiconductor integrated circuit, the semiconductor integrated

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circuit is mounted in the opening, and the semiconductor integrated circuit is connected to the electrode pattern of the base through the plurality of bumps.

Please replace paragraph **[0022]** as follows:

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[0022] In another exemplary embodiment of the present invention, in the piezoelectric device described above, the plurality of bumps formed on the semiconductor integrated circuit are formed at regular intervals at the center portion of the active element surface of the semiconductor integrated circuit.

Please replace paragraph **[0023]** as follows:

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[0023] In another exemplary embodiment of the present invention, in the piezoelectric device described above, a dummy bump is formed on the active element surface of the semiconductor integrated circuit.

Please replace paragraph **[0024]** as follows:

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[0024] In another exemplary embodiment of the present invention, in the piezoelectric device described above, the dummy bump formed on the semiconductor integrated circuit is connected to the electrode pattern on the base.

Please replace paragraph **[0025]** as follows:

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[0025] In another exemplary embodiment of the present invention, the piezoelectric device described above, further includes a layered part on which the piezoelectric resonator is mounted and which surrounds the semiconductor integrated circuit, the layered part including at least two layers including a first layer and a second layer, wherein an opening of the first layer is formed to be larger than an opening of the second layer.

Please replace paragraph **[0026]** as follows:

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[0026] In another exemplary embodiment of the present invention, in the piezoelectric device described above, each of the plurality of bumps formed on the

semiconductor integrated circuit is shaped to have two levels, one having a diameter 0.8 to 0.9 times and the other having a diameter 0.4 to 0.45 times the length of an opening in a pad provided on the active element surface of the semiconductor integrated circuit.

Please replace paragraph **[0027]** as follows:

[0027] In another exemplary embodiment of the present invention, in the piezoelectric device described above, the base includes a ceramic composite substrate.

Please replace paragraph **[0028]** as follows:

[0028] In another exemplary embodiment of the present invention, in the piezoelectric device described above, the plurality of bumps formed on the semiconductor integrated circuit are Au bumps.

Please replace paragraph **[0029]** as follows:

[0029] Another exemplary embodiment of the present invention is a piezoelectric device including a semiconductor integrated circuit and a piezoelectric resonator element included in a package, wherein an opening is formed in the center of a base provided with an input/output electrode pattern is formed, a plurality of bumps are formed at two opposing sides of an active element surface of the semiconductor integrated circuit, the semiconductor integrated circuit is mounted in the center of the opening, and the semiconductor integrated circuit is connected to the electrode pattern through the plurality of bumps by ultrasonic bonding.

Please replace paragraph **[0030]** as follows:

[0030] In another exemplary embodiment of the present invention, in the piezoelectric device described above, a vibration direction of ultrasonic waves applied to the semiconductor integrated circuit is perpendicular to the two opposing sides of the active

element surface of the semiconductor integrated circuit at which the plurality of bumps are formed.

Please replace paragraph **[0031]** as follows:

[0031] In another exemplary embodiment of the present invention, in the piezoelectric device described above, a printing direction of the electrode pattern on the base and a vibration direction of ultrasonic waves applied to the semiconductor integrated circuit are the same.

Please replace paragraph **[0032]** as follows:

[0032] In another exemplary embodiment of the present invention, in the piezoelectric device described above, each of the plurality of bumps formed on the semiconductor integrated circuit is shaped to have two levels, one having a diameter 0.8 to 0.9 times and the other having a diameter 0.4 to 0.45 times the length of an opening in a pad provided on the active element surface of the semiconductor integrated circuit.

Please replace paragraph **[0033]** as follows:

[0033] In another exemplary embodiment of the present invention, in the piezoelectric device described above, each of the plurality of bumps formed on the semiconductor integrated circuit is shaped to have two levels, one being 80 to 90 μm in diameter and 30 to 35 μm in height, and the other being 40 to 45 μm in diameter and 30 to 35 μm in height.

Please replace paragraph **[0034]** as follows:

[0034] In another exemplary embodiment of the present invention, in the piezoelectric device described above, the base consists of a ceramic composite substrate.

Please replace paragraph [0035] as follows:

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[0035] In another exemplary embodiment of the present invention, in the piezoelectric device described above, the plurality of bumps formed on the semiconductor integrated circuit are Au bumps.

Please replace paragraph [0036] as follows:

A32

[0036] In another exemplary embodiment of the present invention, in the piezoelectric device described above, the longitudinal direction of the electrode pattern on the base and a vibration direction of ultrasonic waves applied to the semiconductor integrated circuit are the same.

Please replace paragraph [0037] as follows:

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[0037] In another exemplary embodiment of the present invention, the piezoelectric device described above includes the semiconductor integrated circuit and the piezoelectric resonator element in included in the package, wherein a vibration direction of ultrasonic waves for ultrasonic bonding and for forming bumps on the semiconductor integrated circuit and a vibration direction of ultrasonic waves for performing ultrasonic bonding of the semiconductor integrated circuit to the package are different from each other.

Please replace paragraph [0038] as follows:

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[0038] Another exemplary embodiment of the present invention is a method for manufacturing a piezoelectric device including a semiconductor integrated circuit and a piezoelectric resonator element included in a package, the method may include: a step of forming a metallic bump on the semiconductor integrated circuit; a step of connecting the semiconductor integrated circuit on which the metallic bump is formed to the base by ultrasonic bonding; a step of detecting a height direction of the semiconductor integrated

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circuit during the ultrasonic bonding; a step of mounting the piezoelectric resonator element; and a step of hermetically sealing a metallic lid to the base.

Please replace paragraph **[0039]** as follows:

[0039] Another exemplary embodiment of the present invention is a method for manufacturing a piezoelectric device including a semiconductor integrated circuit and a piezoelectric resonator element included in a package, the method may include: a step of

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forming a metallic bump on the semiconductor integrated circuit; a step of connecting the semiconductor integrated circuit on which metallic bump is formed to the base by ultrasonic bonding; a step of detecting a height direction of the semiconductor integrated circuit during the ultrasonic bonding step; a step of filling an underfill material around the semiconductor integrated circuit so as to cover the entire semiconductor integrated circuit including a rear surface of the semiconductor integrated circuit; a step of mounting the piezoelectric resonator element; and a step of hermetically sealing a metallic lid to the base.

Page 7, line 22, delete current paragraph and insert therefor:

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BRIEF DESCRIPTION OF THE DRAWINGS

Please replace paragraph **[0040]** as follows:

[0040] Figs. 1(A)-(B) are structural diagrams of a piezoelectric device according to

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the present invention;

Fig. 2 is a diagram illustrating the formation of a bump on a wafer of the piezoelectric device of the present invention;

Fig. 3 is a diagram showing the shape of the bump of the piezoelectric device of the present invention;

Fig. 4 is a diagram showing the shape of another bump of the piezoelectric device of the present invention;

Fig. 5 is a process diagram illustrating a flip-chip bonding process of the present invention;

Fig. 6 is a stress distribution map according to FEM analysis;

Fig. 7 is a structural diagram showing another embodiment of the present invention;

Fig. 8 is a structural diagram showing another embodiment of the present invention;

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Fig. 9 is a structural diagram showing another embodiment of the present invention;

Figs. 10(A)-(B) are a plan view and a front view, respectively, showing another embodiment of the present invention;

Figs. 11(A)-(B) are a plan view and a front view, respectively, showing another embodiment of the present invention;

Fig. 12 is a structural diagram showing another embodiment of the present invention;

Fig. 13 is a structural diagram showing a cross-section of a bonded portion of the present invention;

Fig. 14 is a structural diagram showing yet another embodiment of the quartz crystal oscillator of the present invention;

Fig. 15 is an enlarged plan view showing a structure of a portion AR in Fig. 14; and

Figs. 16(A)-(B) are structural diagrams of a conventional piezoelectric device.

Page 8, line 25, delete current paragraph and insert therefor:

DETAILED DESCRIPTION OF PREFERRED EMBODIMENTS

Please replace paragraph **[0043]** as follows:

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[0043] Figs. 1(A)-(B) are structural diagrams of a surface-mount type quartz crystal oscillator according to an embodiment of the present invention.

Please replace paragraph **[0044]** as follows:

[0044] As shown in a plan view of Fig. 1(A) and in a front view of Fig. 1(B), on a first layer of a base 1 consisting of a ceramic insulating substrate having at least three layers and a seal ring of Fe-Ni alloy or the like, stamped to a frame shape, an electrode pattern 3 for forming a connection with a semiconductor integrated circuit (IC chip: hereinafter referred to as the IC chip) 2 is metallized by means of printing by using metal wiring material such as W (tungsten), Mo (molybdenum). On the top thereof, Ni plating and Au plating, etc., are provided.

Please replace paragraph **[0058]** as follows:

[0058] The wafer IC chip 2 is picked up by a nozzle such as an inverted pyramidal collet, is turned over, and is passed on to an nozzle tip of an ultrasonic horn. Then, the IC chip 2 is aligned and is chip-mounted on a mounting area of the base 1 with high precision by a system such as an image recognition system provided in the flip-chip bonding apparatus.

Please replace paragraph **[0066]** as follows:

[0066] As shown in Figs. 1(A)-(B), a configuration in which an opening 16 is formed in the center of the base 1 and the IC chip 2 is mounted in the center of the opening 16 is employed. Thus, when the quartz crystal oscillator 13 is exposed to stress, by this configuration, the stress is evenly applied to the IC chip 2, preventing the stress from concentrating in a specific portion.

Please replace paragraph **[0077]** as follows:

[0077] As shown in Figs. 1(A)-(B), the AT-cut quartz crystal resonator 6 is connected and fixed by the conductive adhesive 9 to mounting electrodes 21 and 22 of the mounting portion 8 provided in the second layer 5 of the base 1.